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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,455	09/18/2003	Keenan W. Franz	AUS920000709US2 (9000/93)	4359

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EXAMINER	
PEIKARI, BEHZAD	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/664,455	FRANZ ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-24,28-30 and 33-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-24,28-30 and 33-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/18/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 21-24, 28-30 and 33-34 in the reply filed on October 6, 2004 is acknowledged. Claim 35 will also be considered as part of the elected invention.

2. With regard to the previous restriction requirement, the following is noted:

(a) In section 1, Group I should have included claim 35.

(b) Section 2, erroneously stated "invention I has separate utility". The sentence should have been, "In the instant case, invention II has separate utility such as the ability to select a configuration without being limited to having at least two address bit signals."

Priority

3. This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a divisional of Application No. 6,760,272, filed December 7, 2000." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

Drawings

4. The drawings are objected to because the size of the reference characters and view numbers does not appear to in accordance with 37 DFR 1.84 (p)(3). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 21-24 and 28-30 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farrell et al., U.S. 5,014,195.

With regard to claim 33, in a microprocessor (*CPU 12, see section A below*) including a controller (*note cache controller 24*) and a multiplexor (*note select logic 38, which performs multiplexing functions*), a method of operating the microprocessor for supporting multiple cache configurations, the method comprising:

operating the controller to generate a first set of at least two address bit signals (*column 2, lines 63-66*) indicative of a first cache configuration (*note that the scope of the claimed "configuration" may include total size, logical partitioning, physical partitions, set associativity, etc.*) among the multiple cache configurations (*note that the address bits help determine, among other things, how many of and what portion of*

memories 26 need to be enabled and accessed, as well as the associativity of the cache, note column 5, lines 13-43);

operating the controller to generate second set of at least two address bit signals indicative of a second cache configuration among the multiple cache configurations (*note that the table in column 7 describes a first cache configuration determined by at least two address bits, a second cache configuration determined by at least two other address bits, as well as a plurality of subsequent configurations determined by different combinations of bits*); and

operating the multiplexor to selectively communicate either the first set of at least two address bit signals or the second set of at least two address bit signals (*note that the address bits described in table 7 are included in the operation of the multiplexing provided by the select logic 38, note column 7, lines 15-17*) to a first memory device (*e.g., a first of cache memories 26*) and a second memory device (*e.g., any other cache memory 26*),

wherein a communication of the first set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the first cache configuration during a boot of the microprocessor (*see section B below*), and

wherein a communication of the second set of at least two address bit signals to the first memory device and the second memory device is an indication of a selection of the second cache configuration during the boot of the microprocessor (*see section B below*).

(A) With regard to the microprocessor *including* the controller and the multiplexor, this was not taught by Farrell et al., whose relevant controller and multiplexor was outside of the microprocessor 12, but still within the data processing system 12. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the cache device 22, or even just the cache controller 24 (which contained the multiplexor 38) into the microprocessor 12, since to have the controller share the chip (1) might have reduced distance delays, thus providing faster communication, (2) might have reduced signal loss associated with longer lines, thus providing more efficient power consumption, (3) might have reduced the number of errors in transmission associated with longer lines and (4) to make integral was not generally given patentable weight, note *In re Larson*, 144 USPQ 347 (CCPA 1965), which was later upheld for electrical circuitry by *In re Tomoyuki Kohno*, 157 USPQ 275 (CCPA 1968).

(B) With regard to either one of two or more cache configurations being established upon boot up, and a second cache configuration being established upon a second boot up (note claim 30), this was not explicitly disclosed by Farrell et al., however, it was well known that operating systems at the time of the invention used their BIOS to initialize memory upon startup. It would have been obvious to one having ordinary skill in the art to establish ones of the various cache configurations in the Farrell et al. system 10 described above, whenever the Farrell et al. system was booted, since (1) memory configuring upon startup was very well known in the art and (2) it

would have allowed the data processing system to know what memory was available and to determine how it should be utilized.

With regard to claims 21-24, 28-29 and 34-35, all of the features of these claims are taught as described above for claims 33 and 30.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (571) 272-4182.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 central hotline at (571) 272-2100.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

12/28/04